REMARKS

(1) Claims 1-9, and 27-30 were pending in the present application. Claim 1 is amended. Accordingly, claims 1-9, and 27-30 are currently pending. No new matter has been added.

(2) The Examiner rejected claims 1-6 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,696,931 to Lum et al. (hereinafter "Lum") over U.S. Patent No. 6,092,149 Hicken et al. (hereinafter "Hicken").

Claim 1 requires, *inter alia*, that the controller "initiates an auto-transfer of the requested data that resides in the cache to the host system; and requests a transfer of the requested data that resides in the mass storage device to the host system, wherein the request of the transfer and the initiation of the auto-transfer occurs **substantially concurrently**" (emphasis added). Lum does not disclose the concurrent or substantially concurrent request of the transfer (of data in mass storage) and the initiation of the auto-transfer (of data in cache). Hicken also does not disclose the concurrent or substantially concurrent request of the transfer and the initiation of the auto-transfer. Accordingly, Applicant submits that claim 1 is patentable over Lum over Hicken, and respectfully request withdrawal of the Examiner's rejection.

Claims 2-6 depend from claim 1. Applicant respectfully submits that these dependent claims are patentable over the cited prior art, not only because of their dependency from claim 1 for the reasons discussed above, but also in view of their novel claim features.

(3) The Examiner rejected claims 8, 27-28, and 30 under 35 U.S.C. § 103(a) as being unpatentable over Lum over U.S. Patent No. 6,141,728 Simionescu et al. (hereinafter "Simionescu").

Claim 8 requires "if a portion of the requested data is in the cache memory and a portion of the requested data is in the mass storage device, transferring the portion of the requested data from the cache memory to the host system **substantially concurrently** (emphasis added) with transferring the portion of the requested data from the mass storage devices to the host system," Claim 27 requires that "said logic means being operable ... **to concurrently cause** (emphasis added) said disk-controller to auto-transfer said cache-hit-portion of said data-blocks corresponding to said data-request from said cache, and to cause said microprocessor to fetch data-blocks corresponding to said cache-miss-portion of said data-request from said disk-device," and Claim 28 requires that "said logic circuit being operable ... **to concurrently cause** (emphasis added) said disk-controller to auto-transfer said first-portion of said data-blocks corresponding to said data-request from said cache, and to cause said microprocessor to fetch data-blocks corresponding to said second-portion of said data-request from said disk-device." Simionescu teaches none of these limitations.

Simionescu merely discloses "If trigger count (trgcount), a value representing the number of sectors available for transfer in a particular cache table entry, reaches zero, a scan for a next segment process 624 is reached and a return is made to the transfer state 623. This process of rescanning and transferring continues until the transfer of all of the requested sectors is completed. At the same time, firmware causes the disk drive to read additional sectors from disk into the cache buffer, and **these additional sectors are located during rescanning and are thereupon automatically transferred to the host** (emphasis added)" (Column 21, lines 16-26). In other words, Simionescu teaches an iterative transfer of the cache content and additional cache sectors that are located during the rescanning to the host. The requested data from a partial cache hit that is in the cache is first transferred to the host. Once the data in the cache has been

transferred "If trigger count (trgcount) ... reaches zero, a scan for a next segment is reached" a rescan is performed to find more of the requested data and continues until all of the requested data has been transferred "This process of rescanning and transferring continues until the transfer of all the requested sectors is complete." Therefore the rescanning and the transfer occur sequentially and not substantially concurrently.

Additionally, Simionescu teaches that the transfer of the requested data from the partial cache hit that is in the disk drive and not in the cache occurs during the rescanning "At the same time ..." (Column 21, line 22) refers to the transfer of data from the disk to the cache and the rescanning and not to "transferring the portion of the requested data from the cache memory to the host system" and "transferring the portion of the requested data from the mass storage devices to the host system" (Claim 8), or "said disk-controller to auto-transfer said cache-hit-portion of said data-blocks corresponding to said data-request from said cache" and "said microprocessor to fetch data-blocks corresponding to said cache-miss-portion of said data-request from said disk-device" (Claim 27), or "said disk-controller to auto-transfer said first-portion of said data-blocks corresponding to said data-request from said cache" and "said microprocessor to fetch data-blocks corresponding to said second-portion of said data-request from said disk-device" (Claim 28). Accordingly, Applicant submits that claims 8, and 27-28 are patentable over Lum and Simionescu, and respectfully request withdrawal of the Examiner's rejection.

Claim 30 depends from claim 28. Applicant respectfully submits that this dependent claim is patentable over the cited prior art, not only because of its dependency from claim 28 for the reasons discussed above, but also in view of its novel claim features.

(4) The Examiner rejected claim 7 under 35 U.S.C. § 103(a) as being unpatentable over Lum in view of Hicken and well-known practices in the art.

Claim 1 requires, *inter alia*, that the controller "initiates an auto-transfer of the requested data that resides in the cache to the host system; and requests a transfer of the requested data that resides in the mass storage device to the host system, wherein the request of the transfer and the initiation of the auto-transfer occurs substantially concurrently." As discussed above, Lum in view of Hicken does not teach or suggest these claim elements. Examiner has not identified and Applicant is unaware of any well-know practices in the art, taken alone or in combination, that disclose the calculation of a new cache counter and pointer values to permit access to data within a cache entry when the first requested data block is not contained within the first block of the cache entry.

Claim 7 depends from claim 1. Applicant respectfully submits that this dependent claim is patentable over the cited prior art, not only because of its dependency from claim 1 for the reasons discussed above, but also in view of its novel claim features.

(5) The Examiner rejected claim 29 under 35 U.S.C. § 103(a) as being unpatentable over Lum in view of Simionescu and well-known practices in the art.

Claim 28 requires, *inter alia*, that "said logic circuit being operable to ... **concurrently cause** (emphasis added) said disk-controller to auto-transfer said first-portion of said data-blocks corresponding to said data-request from said cache, and to cause said microprocessor to fetch data-blocks corresponding to said second-portion of said data-request from said disk-device." As discussed above, Lum in view of Simionescu does not teach or suggest this element. Examiner

has not identified and Applicant is unaware of any well-know practices that disclose the quoted claim limitation.

Claim 29 depends from claim 28. Applicant respectfully submits that this dependent claim is patentable over the cited prior art, not only because of its dependency from claim 28 for the reasons discussed above, but also in view of its novel claim features.

(6) The Examiner rejected claim 9 under 35 U.S.C. § 103(a) as being unpatentable over Lum in view of Simionescu and U.S. Patent Publication 2001/10014929A1 Taroda et al. (herein after "Taroda").

Claim 8 requires "if a portion of the requested data is in the cache memory and a portion of the requested data is in the mass storage device, transferring the portion of the requested data from the cache memory to the host system **substantially concurrently** (emphasis added) with transferring the portion of the requested data from the mass storage devices to the host system." As discussed above, Lum over Simionescu and Taroda does not teach or suggest this element.

Claim 9 depends from claim 8. Applicant respectfully submits that this dependent claim is patentable over the cited prior art, not only because of its dependency from claim 8 for the reasons discussed above, but also in view of its novel claim features.

(7) In view of the above, Applicant respectfully submits that the application is in condition for allowance and request that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner please contact Applicants' attorney at the address below. No fee is believed due in connection with this filing. However, in

the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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